Dynamic chip stencil lithography

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Chapter 1

Dynamic stencil deposition

This chapter is discussing the background of the project for the design of a dynamic stencil lithography setup. First a description of the project is given. Thereafter, prior art is discussed and compared with our developed concept.

1.1 Project description

Recent developments are going towards miniaturized devices and structures in the sub-micrometre range. Advanced photolithography is using deep ultra-violet (DUV), x-ray, electron beam, or ion beam exposure systems. Today we know complementary patterning methods like the scanning probe lithography [24], nano-imprint lithography [4], micro-contact printing [14], Dip-Pen lithography [18], Nanoscale dispensing (NADIS) [13] and the shadow mask technique [11].

The stencil lithography technique is based on defining patterns under vacuum by evaporation of a material through stencil apertures. A stencil (also called a shadow mask) consists of a silicon nitride (SiN) membrane which is mounted onto a Silicon (Si) frame. The side length of such a stencil chip is a couple of millimetres (typically 6 or 10mm). The membrane contains apertures with diameters on the order of micro- and nanometres. A typical example of such a mask is shown in Figure 1.1.

The stencil is masking or shadowing most of the underlying substrate. Only the material that passes through the membrane apertures is deposited on the substrate. This technique

![Figure 1.1: Section through a stencil: Silicon wafer as frame with a free standing silicon nitride membrane. The membrane contains micro- and nanometre sized apertures.](image-url)
allows defining micro- and nanometre sized structures. It has the advantage of allowing direct patterning. No additional fabrication steps such as lithography or etching are necessary. This limits the sources of contamination on the substrate. When bringing the stencil only in proximity and not in contact with the substrate, a further advantage is that physical scratching is completely avoided. Figure 1.2 shows a static setup where the nanostencil is not moved during evaporation. Any non-zero gap causes blurring of the deposition, which is defined and discussed in the next section.

The static mode is limited: It is not possible to deposit patterns with a closed geometry, such as a ring. The dynamic mode (Figure 1.3) on the other hand allows a ring to be deposited by moving the stencil in a circle. Furthermore, depositions with varying thickness can be made by changing the speed of the stencil.

Based on a previous works of Frédéric Chautems [3], Jurgen Duivenvoorden [5] and Hans-Christian Schneider [21], the goal of this Semester Project is to develop a setup that allows dynamic stencil lithography at chip level. Such a setup is shown in Figure 1.4. It contains an xy-stage with a holder that allows fixing a stencil on the xy-stage. The stencils parallelism to
the substrate is induced by simply placing the substrate on the stencil. The gravitation forces will ensure parallelism. Three piezo actuators that move in z direction are then approaching the substrate from underneath.

Contact is detected and thus the initial point for the movement is determined (gap = 0). Now, all piezos can move to a predefined distance of gap. Actually, all actuators together allow controlling the gap distance and the angle between stencil and substrate. These movements are generated by a controller which is outside the vacuum environment.
1.2 State of the art in Stencil Lithography

In 1996 K. Ono et al. presented a new deposition technique based on shadow masks with membranes in $\text{Si}_3\text{N}_4$ [17]. With two piezo actuators they were able to do dynamic depositions with the goal to produce small tunnel junctions. Their setup had one degree of freedom during deposition and thus was able to create lines. Figure 1.5 shows the schematic setup that they were using.

IBM Zurich Research Laboratory did integrate in 1999 stencil-like apertures onto an atomic force microscope (AFM) cantilever [12], which is shown in Figure 1.6. These apertures were made by focused ion beam (FIB). They were able to deposit structures well below 100nm. The AFM tip fulfilled two tasks: it was responsible for the gap control and the in situ analysis of the deposited structure.

Racz et al. [19] fixed a shadow mask on an xy-stage. This stage was movable over a full wafer of 100mm with a resolution of 1nm. The goal was to obtain nano-size features from micron-size stencil apertures. Multiple layers of two different materials are deposited alternating. After the deposition one of the materials is lifted off, leaving only the second material in places where it did not overlap the first one. They did know that during deposition the apertures do gradually clog. The displacement of the mask needs between evaporations needs to be the desired feature thickness plus the thickness of clogging of the aperture. The above mentioned fabrication process is made visible in Figure 1.7.

Over the years, there were more and more publications in this field of research. Development of a reliable dynamic stencil setup became the goal of different groups. In 2005 the Nanoscience Group of the University of Cambridge (GB) published their intermediate results on their way to make the stencil technique a universal tool for nanoscience [6]. The gap is controlled in closed loop with laser beam deflection detection (AFM like). One of their goals for the future is to implement a AFM tip on the stencil. This should allow alignment to existing structures prior to deposition and in situ analysis of the deposition results (see Figure 1.8).

A further development has been made by IBM in 2005. They published an all-in-one static
and dynamic nanostencil setup with integrated atomic force microscope, scanning tunneling microscope and a four-point-probe [27]. All these different tools – nanostencil, AFM, STM and four-point-probe – are being integrated onto a carousel. The substrate itself is mounted on a xyz-table which allows doing dynamic depositions. A schematic of this machine is shown in Figure 1.9.

It is our idea to develop a setup which has its origin in the work of Ono et al.. The goal is to create a setup that allows using batch produced stencils. These stencils need to be easily exchangeable. For the moment, no inspection tool – like SPM or AFM – is planned to be integrated. This might be a very interesting option for later developments. The final setup should consist of a low-cost, high accuracy tool that allows rapid prototyping of micro- and nanometre sized structures. The definition of such structures should be possible by the use of a simple deposition setup and our developed tool, even in a low-tech environment.

A possible field of dynamic stencil applications might be combinatorial materials science. Since structures in integrated circuits – for example in MOS transistors – are getting smaller, SiO$_2$ is no longer a sufficient gate isolator. That is just one example for which new combinatorial materials with advantageous properties are searched. In this field the dynamic stencil might be a promising application for MEMS tools. Instead of producing “material libraries” with a rotational table [25], as shown in Figure 1.10 and Figure 1.11, this could be done by use of stencils.

Figure 1.6: Schematic of apertures integrated onto an atomic force microscope (AFM) cantilever: Material is evaporated by means of physical vapor deposition (PVD). From the material source (A) it is deposited trough micron- and nano-sized apertures on and AFM cantilever (D) onto a substrate (E). The tip (D) is responsible for the gap control between substrate and mask and serves to inspect depositions in situ. Source [12]
Figure 1.7: Nanopositioner-translated shadow mask evaporation and lift-off are used to form nanometre inter-embedded metal features (a) to (e). Two thicknesses of lines are shown in (e). Source [19]

Figure 1.8: Schematic of setup: (1) sample mounted on the approach and alignment assembly, composed of inchworm, flexure stage, and two inertial sliders (x-y and tilt); (2) stencil mask cantilever; (3) e-beam evaporator; (4) laser; (5) quadrant photodiode; (6) light source; (7) optical microscope with CCD camera. Source [6]
Figure 1.9: Carousel mechanism using a snapper for repositioning consisting of xyz-stage, substrate, stencil mask mounted on carrier block on a carousel. Source [27]

Figure 1.10: Schematic of the combinatorial mechanism by Yamamoto et al.: The mechanism consists of three changeable targets, a fixed substrate and a rotating mask system placed between them. The mask has three patterns. Source [25].
Figure 1.11: The procedure of making a ternary composition spread film with the combinatorial mask by Yamamoto et al.: The mask pattern is supposed to move above the plane. The color density expresses the thickness of the film on the substrate. Source [25].
1.3 Project outline

The project is divided into three different parts. Three students are working on the following elements of the stencil lithography system:

Aris Maroonian’s part consists of improving the Z actuators for controlling the gap between stencil and substrate (see Figure 1.4). This involves designing and fabricating new piezo actuators, as well as characterizing their performance. Also, the contact detection between the actuators and the substrate holder needs to be tested.

Patrice Lauber is designing a LabVIEW interface to control the dynamic stencil system. This computer program will output the necessary voltages to control all the piezo actuators. It must also measure the contact of the Z actuators and the substrate.

Finally, the goal of the present semester project is to improve the fixation of the stencil, as well as to design stencils for various applications. The use of electrostatic force to hold the stencil in place will be investigated. Compatible chip stencils will be made that can exploit the advantages of the dynamic mode.

In Chapter 2, the design of a new stencil holder is presented. Its performance is characterized in Chapter 3. Several applications for stencil lithography are described in Chapter 4, together with the respective designs we used in our stencils. This report then gives a conclusion and recommendations for future work.
Chapter 2

Stencil chuck

As shown in the introduction, our system uses a chip stencil that is held in close distance to a substrate, and moved laterally to deposit patterns on the substrate. The stencils are made in batches from Si wafers and need to be fixed to the xy-stage. In this project we developed a stencil chuck which uses electrostatic force for securing the stencil to its holder.

![Side view of stencil and substrate with respective holders](image1)

Figure 2.1: Side view of stencil and substrate with respective holders

2.1 Previous work

In previous work done at EPFL/LMIS, adhesives or springs were used to hold the stencil. But gluing the stencil to the xy-table is not practical. During evaporation, the material will

![Clogging of membrane apertures](image2)

Figure 2.2: Clogging of membrane apertures. Source [21]
accumulate not only on the membrane surface but also on the side walls of any aperture in the membrane. If the pattern dimension is in the same order of magnitude as the stencil membrane thickness, the evaporated metal tends to clog the stencil. If the stencil was glued to the xy-table, changing it would be difficult and one would risk damaging the fragile setup.

Mechanical clamping is not trivial either. The most important restriction is that no object must extend past the upper surface of the stencil. Figure 2.3 shows a stencil chuck that has two springs acting in the x and y directions. The stencil was not secure however, because its edges were inclined due to the cleaving process. The spring force would cause the stencil to jump out of its position. Another project used stencils with pyramidal edges and a corresponding recess in the chuck (Figure 2.4). The fabrication of the stencils is more complicated, as simple cleaving or saw dicing is not possible. The dimensions of the stencil and the chuck must be adjusted very well so that the stencil just slightly protrudes out of the chuck. In both designs, the fixing of the stencil is a manually difficult task.

Electrostatic clamping was tried, with unsatisfactory results. An interdigitated geometry with various electrode widths was tested. One chuck with a hole of $3 \times 3$ mm is shown in Figure 2.5. The electrodes consist of a $0.7 \mu$m layer of aluminium. They are sealed by a layer of polyimide with a thickness of $2.3 \mu$m.

Out of dozens of fabricated stencils, only a few worked and required a voltage of several hundred volts. Another problem was the choice of aluminium for the electrodes, on which it is difficult to solder wires for the voltage supply. One goal of the present project is to investigate and improve the geometry and material composition of the electrostatic chuck.
2.2 Requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compatibility</td>
<td>Size must fit on existing xy-stage.</td>
</tr>
<tr>
<td></td>
<td>Light-weight in order not to deform the xy-stage.</td>
</tr>
<tr>
<td></td>
<td>No part must interfere with substrate.</td>
</tr>
<tr>
<td>Simple operation</td>
<td>Quick manual fixation and release of stencil.</td>
</tr>
<tr>
<td>Sufficient clamping force</td>
<td>Clamping force must be higher than both the weight of stencil and the acceleration force due to x-y displacement.</td>
</tr>
</tbody>
</table>
2.3 Possible solutions

2.3.1 Wafer-electrode electrostatic chuck

An electrostatic chuck for an entire wafer was developed at IBM by Wardly in 1973 [22]. This chuck consisted of a single electrode, with the wafer being the other electrode of the capacitor. The wafer is separated from a metal electrode by a thin insulator. An alternating voltage is applied to the electrode, to avoid accumulation of charges in the dielectric. This setup would not be useful in this project as the wafer must have a metallic electrode on it for the ground connection.

2.3.2 Interdigitated electrodes electrostatic chuck

To avoid charge accumulation with DC voltages, bi-polar interdigitated electrodes can be used. The fundamentals of such a chuck were investigated by Asano et.al. [2]. They made electrode configurations as shown in Figure 2.7, for use with a full-size wafer. The observed force was higher for the interdigitated electrodes. Also, narrower spacing of electrodes showed a stronger force up to a point where current leakage and breakdown become problematic.
2.3.3 Force between electrodes of a capacitor

When a planar capacitor is charged, the electrodes will receive charges $+q$ and $-q$. Looking at the electric field generated by one electrode, Gauss’ Law states the relationship between $q$, the flux $\Phi$ and the electric field $E$:

$$\Phi = \oint_S E \, dA = \frac{q}{\epsilon_0}$$

where $dA$ is the differential area on the surface $S$ enclosing the electrode. We assume that the field is constant and perpendicular to the surface and approximate the electrode by a plane of total surface $2A$ (front- and backside).

$$E \oint_S dA = 2AE = \frac{q}{\epsilon_0}$$

where $\epsilon_0$ is the permittivity of free space. The total field magnitude $E_{tot}$ is the sum of the fields of each electrode. The electric field can be approximated by the voltage $V$ divided by the distance $d$.

$$E_{tot} = 2E = \frac{q}{A\epsilon_0} = \frac{V}{d}$$

$$q = \frac{A\epsilon_0V}{d}$$

The electrostatic force is the product of charge and field magnitude:

$$F = qE_{tot} = \frac{q^2}{2A\epsilon_0} = \frac{\epsilon_0AV^2}{2d^2}$$

Introducing the definition of the capacitance $C$:

$$C = \frac{A\epsilon_0\epsilon_r}{d}$$

$$F = \frac{CV^2}{2d} \quad (2.1)$$

It should be noted that this approximative equation assumes that the spacing between electrodes is bigger than the spacing between one electrode and the stencil. Also, the electric field will in reality not be homogeneous at the edge of the electrodes.
2.4 Design of a new electrostatic chuck

Applying equation (2.1) to our case, there are some considerations to be taken into account: the voltage $V$ is half of what we apply to the electrodes ($V_a$), as can be seen in Figures 2.6 and 2.8. The capacitor surface $A$ is the surface of the chuck minus the spacing between the electrodes.

The capacitor is made of more than one dielectric. There is an insulating layer on the chuck, of thickness $d_{\text{ins}}$ and relative permittivity $\varepsilon_{\text{ins}}$. The Si$_3$N$_4$ layer (with $d_{\text{SiN}}$, $\varepsilon_{\text{SiN}}$) on the stencil is also introduced for the sake of completeness, but its influence on the capacitance is negligible. Also, there is a vacuum between chuck and stencil due to wafer curvature and dust, as is shown on Figure 2.9. The total capacitance is as follows:

$$C = \frac{1}{\sum \varepsilon_i} = \frac{A\varepsilon_0}{d_{\text{ins}}\varepsilon_{\text{ins}} + d_0 + d_{\text{SiN}}\varepsilon_{\text{SiN}}}$$  \hfill (2.2)

The capacitance between electrodes and stencil is calculated by (2.2), using the parameters in Table 2.1, which gives 71pF.

The voltage required for a clamping force of 45mN is:

$$V_a = 2\sqrt{\frac{2F}{C}(d_{\text{ins}} + d_0 + d_{\text{SiN}})} = 248V$$
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$</td>
<td>Contact area of stencil and chuck electrodes</td>
<td>84</td>
<td>mm$^2$</td>
</tr>
<tr>
<td>$d_{ins}$</td>
<td>Thickness of dielectric material</td>
<td>2</td>
<td>µm</td>
</tr>
<tr>
<td>$d_{SiN}$</td>
<td>Thickness of Si$_3$N$_4$ layer on stencil</td>
<td>0.1</td>
<td>µm</td>
</tr>
<tr>
<td>$d_0$</td>
<td>Distance due to wafer curvature and dust, estimated</td>
<td>10</td>
<td>µm</td>
</tr>
<tr>
<td>$m_s$</td>
<td>Mass of stencil, $10 \times 10 \times 0.38\text{mm}^3 \times \rho_{Si}$</td>
<td>0.09</td>
<td>g</td>
</tr>
<tr>
<td>$F_a$</td>
<td>Lateral accelerating force on the stencil, estimated $5m_sg$</td>
<td>4.5</td>
<td>mN</td>
</tr>
<tr>
<td>$\mu_s$</td>
<td>Static friction coefficient between polyimide and Si$_3$N$_4$, est.</td>
<td>0.1</td>
<td></td>
</tr>
</tbody>
</table>

Table 2.1: Parameters for calculating electrostatic force

As far as the electrode spacing is concerned, the critical factor is the breakdown field of the SU-8 film, which is 112V/µm. The breakdown field strength for the underlying SiO$_2$ is not influential, as it is of the order of 1kV/µm. For a voltage of 1kV, a minimum distance of 8.9µm must be guaranteed. With some safety margin, we use 20µm here. This spacing is so small compared to the total area that it can be neglected for the calculation of the force.

### 2.4.1 Chuck fabrication

Chucks were made on an Si wafer with copper electrodes of a total area of 84mm$^2$ for each chuck. One electrode design is shown in Figure 2.10. The copper was covered with a SU-8 resist for insulation. Polyimide has not been used as it is difficult to handle and gives results that are hard to reproduce. The SU-8 has openings at the the pads at the bottom for soldering wires.

Another resist was spun on the wafer for protection during laser cutting of the center holes and dicing. The details of the process are described in Section A.2 of the appendix. After the clean-room processing, wires were soldered to the contact pad.

A single stencil chuck is shown in Figure 2.12. 32 chucks with various electrode configurations were made. They will be characterized in the next chapter. The number of electrode fingers made was 2 (Fig. 2.11), 4, 14 (Fig. 2.10), 26 and 60.
Figure 2.10: Chuck with 14 alternating electrodes (14 “fingers”). Outer dimensions are $11 \times 13\text{mm}^2$, inter-electrode spacing is exaggerated.

Figure 2.11: Chuck with two simple, non-interdigitated electrodes. Inter-electrode spacing is exaggerated.
2.5 Integration with dynamic stencil system

One of the electrostatic chucks was fixed to the existing xy-stage by means of a double-faced adhesive tape. The two wires share a connector and cable with the wires for the piezo voltage. The cable is then brought out of the vacuum chamber through an airtight connector.
Figure 2.13: General view of the dynamic stencil deposition system, with the electrostatic chuck fixed in the center. One z-actuator is missing.

Figure 2.14: Detail view of the xy-stage. A test stencil with no membranes has been put on the chuck. The x and y piezo actuators can be seen at the left and bottom border of the image.
Chapter 3

Characterization

We will examine the results of the fabrication process here. The maximum applicable voltage is measured, which may depend on fabrication parameters that are difficult to control. Then, each chuck will be tested individually to establish a relationship between applied voltage and electrostatic force.

3.1 Test structures on chuck wafer

Apart from the stencil chucks, test structures were made on the same wafer. They are used to measure the etching characteristic of the copper and the breakdown voltage of the dielectrics (SU-8 and SiO2). These structures consist of one common electrode being in close distance to 4 other electrodes, with spacing between 1 and 20μm. One such structure is shown in Figure 3.1, with the bare copper shown in green and the copper covered by SU-8 shown in blue.

Figure 3.1: Copper test structure
3.1.1 Copper under-etch

With the use of an optical microscope, the effective spacing between the electrode was measured. The values are compared to the computer design dimensions in Figure 3.2. Especially for small gaps, a definitive measurement was difficult, as the etching was not homogeneous in these cases. For a nominal spacing bigger than 5µm, it can be said that the gaps are about 7.5µm larger than designed.
3.1.2 Breakdown voltage

Next, the maximum usable voltage was determined. Wires were soldered to the electrode pads and a DC voltage was applied. The voltage was constantly increased until breakdown occurred, which was visible and audible as small sparks. As expected, the SU-8 in the gap between two electrodes would break down, the arc would burn some of the SU-8 and melt the copper, as shown in Figure 3.4.

Breakdown also occurred in the middle of the bare copper contact pad (Figure 3.5). This is most likely due to a breakdown of the SiO$_2$ under the copper electrode. When the dielectric strength of this layer is exceeded, arcing can occur at the weakest point, leaving a crater.

The breakdown voltages for different electrode spacing are shown in Figure 3.6. Breakdown through SiO$_2$ happens at around 1.3kV, naturally independent of spacing as it occurs not at the gap. The breakdown of SU-8 approximately follows a linear relationship. A linear regression shows that $V_{\text{breakdown}} \approx 66 \cdot d_{\text{spacing}} [\mu m]$, meaning that the dielectric strength of the SU-8 is 66V/µm. The value given by the manufacturer is almost twice as high. The difference can be explained by the fact that the deposition of th SU-8 was not perfect, especially at the edge of the electrodes. If there are cracks or pores in the material, the breakdown can occur partly
through air, which as a limiting voltage as low as about 3V/µm [7].

It can be concluded that for the stencil chucks made in this project, any voltage below 1kV is safe if the chuck has no defects. The spacing between electrodes is nominally 20µm, therefore the voltage is limited to 1.3kV, the breakdown voltage of the SiO₂ layer. It is advisable to test the electrostatic chuck before integrating it with the stencil lithography system to detect insufficient copper etching or defects in the dielectric materials.
Finally, the voltage necessary to hold the stencil in place must be measured. Instead of measuring the static friction force due to the electrostatic attraction, a simpler and more accurate method was used: We measured the voltage necessary to lift the chuck, when pulling the stencil upwards. A small weight was attached to the chuck to bring the total mass to 2.4g. If the electrostatic force is greater than $F_e = mg = 24\text{mN}$, we will be able to lift the chuck.

Figure 3.8 shows the voltages measured for 30 different chucks, sorted according to the number of electrode fingers. These results show that while there are some variations between the different electrode configurations, it cannot be said that densely interdigitated electrodes are
better than non-interdigitated ones.

According to the equation (2.2), the theoretical value for the voltage is 181V for the weight used. This was a pessimistic estimation, most likely the distance $d_0$ due to dust and wafer curvature was over-estimated.

We have measured both the maximum voltage ($\approx 1$kV) and the necessary voltage for a force more than two times the weight of the stencil ($< 160$V). We can conclude that we have the possibility to decrease the electrode size. A higher voltage is then necessary for the same force. This would allow us to make smaller stencils or stencils with more useful membrane surface.
Chapter 4

Stencils

4.1 Previous work

Stencils had already been made in previous projects in the same size as is used here. The patterns included circular holes of different diameters, as shown on Figure 4.1.

Figure 4.1: Backside view of the stencils previously made at EPFL. The pitch of the apertures varies from 1.5 to 10µm. Source [20]
4.2 Requirements

The stencil must fit the chuck designed in the previous chapter, that means it must have a size of $10 \times 10 \text{mm}^2$. It should have one or several membranes in the central region of $4 \times 4 \text{mm}^2$. A low-cost stencil lithography systems requires that the stencils be made in batches, with as many stencils per wafer as possible.

4.3 Design

A wafer coated on both sides with 100nm of silicon nitride (SiN) was used. First, the front side SiN is patterned by e-beam. Apertures for different applications were made, these are described in the next section. On the back side, the membranes are then defined by etching the SiN. Finally, the silicon is etched with KOH to expose the top side membranes. The process is described in more detail in appendix A.3.

For making the stencils, an existing mask was used. This mask has 9 membranes per stencil. Figure 4.2 shows a section of four stencils. The dark areas inside the membrane squares indicate the usable area of the membrane. This is limited by the inclined walls created by the KOH etch, and also by the size of the hole in the stencil chuck.

4.4 Applications

The aperture patterns made in this project include dots and line slits of different sizes, wires (line slits with pads), crossing wires, and single-electron transistors.
4.4.1 Dots and lines

Some chips were made with circular and square holes in sizes in the range of 50 to 200nm. These can be used in dynamic mode to deposit arbitrary shapes. Ring shapes, for example, can be done which are not possible in static mode.

We also made slits that have widths in the same magnitude, and lengths varying from one to 10 microns. When used in dynamic mode, these slits can make films with varying thickness. The thickness of the film is inversely proportional to the speed of the stencil’s movement, as shown in Figure 4.4.
4.4.2 Wires and crossed wires

When deposited in thin layers, Bismuth is a semiconductor rather than a semimetal. This was suggested for example in 1966 by Ogrin et.al. [16], but for a long time these and other experiments did not provide compelling evidence. In 1993, experiments by Hoffman et.al. showed a clear decrease (for $T < 100$K) of electron and hole mobility for thin films, compared to bulk Bi [10]. The critical dimension for the semimetal-to-semiconductor transition (SMSC) is in the order of 50nm.

Stencil deposition can be used to make structures in the necessary sizes. These nano-structures can then be characterized by measuring resistivity, Hall effect or other properties.

A practical problem when working with Bismuth is the oxidation that occurs in a normal atmosphere. This makes it difficult to electrically connect the films or wires, after the substrate has been taken out of the deposition chamber. By using a dynamic stencil system, a non-oxidising metal such as gold can be deposited on top of the bismuth without removing the substrate from the vacuum chamber. When designing the layout of wires and pads, care must be taken to avoid any unwanted overlapping, taking into account the maximum displacement of the xy-stage (about 200µm).

We have made stencils that have a single wire such as shown on the upper right in Figure 4.3 (the apertures for the gold pads are not shown). It is also interesting to deposit overlapping wires of bismuth with dimensions below and above the critical size. This can be done using a different pattern (Fig 4.5). An evaporation of bismuth is made, then the stencil is moved to the left. A second Bi evaporation will make a wire overlapping the first one. Finally, the stencil is moved upwards, and gold is deposited. The gold pads have a size of 100 × 200µm for simple contacting by wire bonding, which is widely used for integrated circuits.
Figure 4.6: SEM image of a membrane with wire apertures of different widths, with two pad apertures each

Figure 4.7: Detail view of one wire. Length: 1μm, width: 100nm
4.4.3 Single electron transistor

A single electron transistor (SET) consists of a small metallic dot (the island), forming two tunnel junctions with a source and drain electrode.

Because the island is very small, the discreteness of electrical charge becomes apparent. An electron tunnelling from the source electrode on to the island will change the potential of the island. Given a sufficiently small capacitance, this change in potential will prevent another electron from tunnelling. The tunnelling current is thus stopped and the increasing resistance is called a Coulomb blockade. The electrical potential can be changed with the gate electrode which is capacitively coupled to the island. Like in a field-effect transistor, the current from source to drain can be controlled by the potential of the gate electrode.

To make an SET, it is necessary to deposit the island (using aluminium for example), to let a layer of oxide form on it, and then to deposit the source and drain electrodes overlapping the island. The source and drain metal on the other hand should not be covered with oxide, otherwise electrical contact is again made difficult. We therefore need a process that allows to change the position of the deposition for the overlap at the island, and for depositing gold pads.

SETs have been made in static mode by changing the angle of the evaporation crucible relative to the stencil. One such transistor made at EPFL is shown in Figure 4.9. Another SET in Figure 4.10 uses niobium for the source and drain leads, which has interesting superconducting properties [8]. Again, the dynamic mode offers the possibility of making several depositions at different positions, including gold contact pads that are easier to connect.
Figure 4.9: SEM image of a single electron transistor made in static mode.

Figure 4.10: A single-electron transistor made in static mode. The island is made from aluminium, source and drain are made from niobium. Source [9]
Chapter 5

Conclusion and outlook

The concept of an electrostatic chuck for chip stencils has been proven to work. We can use voltages below 200V and achieve a reliable clamping of the stencil. This means that no problems are to be expected when using standard wire insulation. For the voltage supply of the chuck, we can therefore use the same cable and vacuum chamber connector as for the piezo control.

Handling of the stencil system is very simple: with the supply voltage turned off, place and align the stencil on the chuck. When the voltage is turned on, the stencil will stay in place even if the whole system is moved or turned upside down.

Various chip stencils (10 × 10mm²) were made. We have shown several applications that can benefit from dynamic stencil deposition, and we have designed and fabricated appropriate stencil patterns. In a future project, these patterns can be improved and tested with the evaporation of several metals such as bismuth or aluminium.

Future improvements for the stencil holder can also be made: As has been shown in Chapter 3, we have some headroom between the necessary voltage for a typical force, and the maximum voltage determined by breakdown. If the same mask for the KOH etch of the stencils is to be kept, the electrodes of the chuck can be made smaller. This means that the central hole in the chuck can be made bigger to make use of the most membrane area.

Also, the measurements have not shown a significant advantage of using interdigitated electrodes vs. two simple paired surfaces. While the fabrication process does not differ for the two configurations, the non-interdigitated design loses less surface area to the spacing, and is less sensitive to damage of the copper by scratching.

While the stencil chuck has been shown to work in the deposition system, the system could not be used for a test of dynamic or static deposition. The piezo actuators for the control of the z distance were not ready at the time of this writing.
5.1 Acknowledgments

Most importantly I’d like to thank my supervisors for their guidance during this Semester Project. Marc A.F. van den Boogaart supported my in the beginning of the project, and Veronica Savu has guided and motivated me for the most part of this work. My thanks go to Prof. Jürgen Brugger who has made this project possible; and to all the members of the LMIS1 laboratory for helpful suggestions and critical questions.

The following people deserve credit for helping me with the various fabrication steps: Claude Amendola doing the laser cutting of the chucks after giving helpful advice on the design, and Guillermo Villanueva, who did the next fabrication step, namely dicing of the chip chucks. Further thanks go to Georges-André Racine, Jean-Marie Voirol and the rest of the CMI staff for their help and advice in the cleanroom.

Finally I would like to thank Patrice Lauber and Aris Maroonian as project collaborators and motivators.

Lausanne, June 17, 2008
Stephan Walter
Appendix A

Fabrication processes

A.1 Properties of materials

<table>
<thead>
<tr>
<th></th>
<th>density [g/cm³]</th>
<th>relative permittivity</th>
<th>breakdown field [V/µm]</th>
<th>source/comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>2.33</td>
<td>11.7</td>
<td></td>
<td>[1]</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>7.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiO₂</td>
<td>4.2</td>
<td>1000</td>
<td></td>
<td>[15]</td>
</tr>
<tr>
<td>SU-8</td>
<td>4.1</td>
<td>112</td>
<td></td>
<td></td>
</tr>
<tr>
<td>air</td>
<td>1</td>
<td>3</td>
<td></td>
<td>[7]</td>
</tr>
</tbody>
</table>
### A.2 Fabrication of stencil holder

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ø100mm Si/SiO₂ wafer (SiO₂ 100nm)</td>
<td></td>
</tr>
<tr>
<td>Cu 1µm</td>
<td>e-beam evaporation</td>
</tr>
<tr>
<td>resist spinning, exposure (mask 1), wet etch, resist removal</td>
<td></td>
</tr>
<tr>
<td>SU-8 deposition, open contacts (mask 2)</td>
<td></td>
</tr>
<tr>
<td>spin resist for protection</td>
<td></td>
</tr>
<tr>
<td>cut membrane via by laser</td>
<td></td>
</tr>
<tr>
<td>dicing</td>
<td>remove protective resist</td>
</tr>
</tbody>
</table>

![Figure A.1: Stencil chuck process](image)

We started with a wafer that already had an oxide layer, which we need for electric insulation. The copper was etched manually in a bath. After a few minutes, the wafer was taken out of the etch bath to measure the thickness. This process leads to some under-etch of the copper, as described in Section 3.1.1.
Figure A.2: Mask 1 for copper etch (to scale)
Figure A.3: Mask 2 for SU-8 openings (to scale)
### A.3 Fabrication of stencils

<table>
<thead>
<tr>
<th>Action</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frontside: spin ZEP520A photoresist (180nm)</td>
<td>e-beam patterning of membrane structures</td>
</tr>
<tr>
<td>Frontside:</td>
<td>SiN dry etch with $\text{C}_2\text{F}_6$</td>
</tr>
<tr>
<td>Backside:</td>
<td>spin resist</td>
</tr>
<tr>
<td>Backside:</td>
<td>expose with mask 3</td>
</tr>
<tr>
<td>Backside:</td>
<td>SiN dry etch with $\text{C}_2\text{F}_6$</td>
</tr>
<tr>
<td>Backside:</td>
<td>Si etch by KOH</td>
</tr>
<tr>
<td></td>
<td>Dicing of chip stencils</td>
</tr>
</tbody>
</table>

Figure A.4: Chip stencils process

For the membrane patterning, two different e-beam processes are used. A coarse beam with a resolution of 100nm but a high speed is used for large structures such as apertures for contact pads. The fine beam is slower but has a resolution of 5nm. It is used for the nano-apertures of slits where precision is important.
Figure A.5: Mask 3 for KOH etch (to scale)
Bibliography


